MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

TAO1221 – COMPUTER ARCHITECTURE AND ORGANISATION

(All sections / Groups)

12 MARCH 2019
9.00 a.m. – 11.00 a.m.
(2 hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages including cover page with 5 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

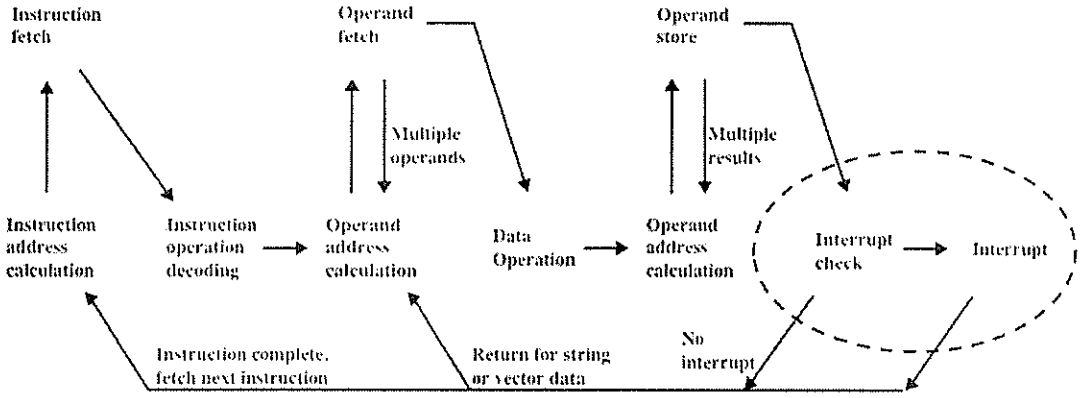
(a) (i)Illustrate the structure of IAS (Institute of Advanced Studies) computer. [1 mark]

(ii) Briefly describe **FOUR (4)** main components in IAS computer. [2 marks]

(b) Define Moore's Law and identify **FIVE (5)** consequences of Moore's Law. [3 marks]

(c) Discuss **THREE (3)** key concepts of von Neumann architecture. [1.5 marks]

(d) Given the following instruction-cycle-with-interrupt state diagram, describe the processes for *instruction fetch*, *operand address calculation*, *data operation*, *operand store*, and *interrupt*. [2.5 marks]



QUESTION 2

(a) Briefly discuss **THREE (3)** types of buses in system bus. [1.5 marks]

(b) Given a scenario where 8 instructions take 5 time units to complete each stage of execution, and each instruction has a number of 9 stages, namely FI, DI, D2, CO, FO, EI, EX, MO and WO.

(i) Draw a timing diagram for the instruction pipeline operation described in the given scenario. [3.5 marks]

(ii) Calculate the total time required to complete the execution of all the instructions without using pipelining. [1 mark]

(iii) Calculate the total time required to complete the execution of all the instructions using pipelining. [1 mark]

(iv) Calculate the speedup factor for the instruction pipeline compared to the execution without the pipeline. [1 mark]

(c) Explain **TWO (2)** basic tasks performed by a control unit. [2 marks]

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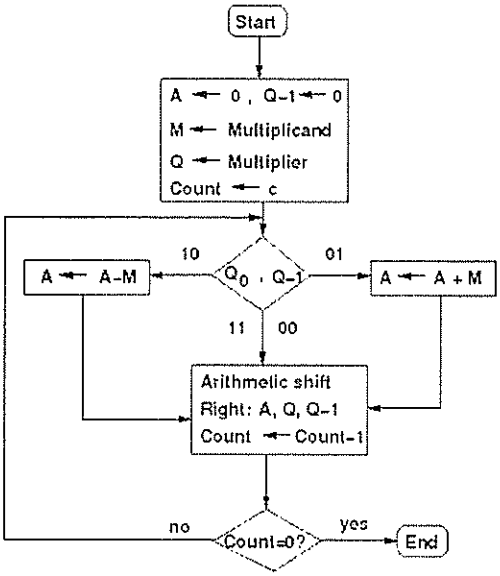
QUESTION 3

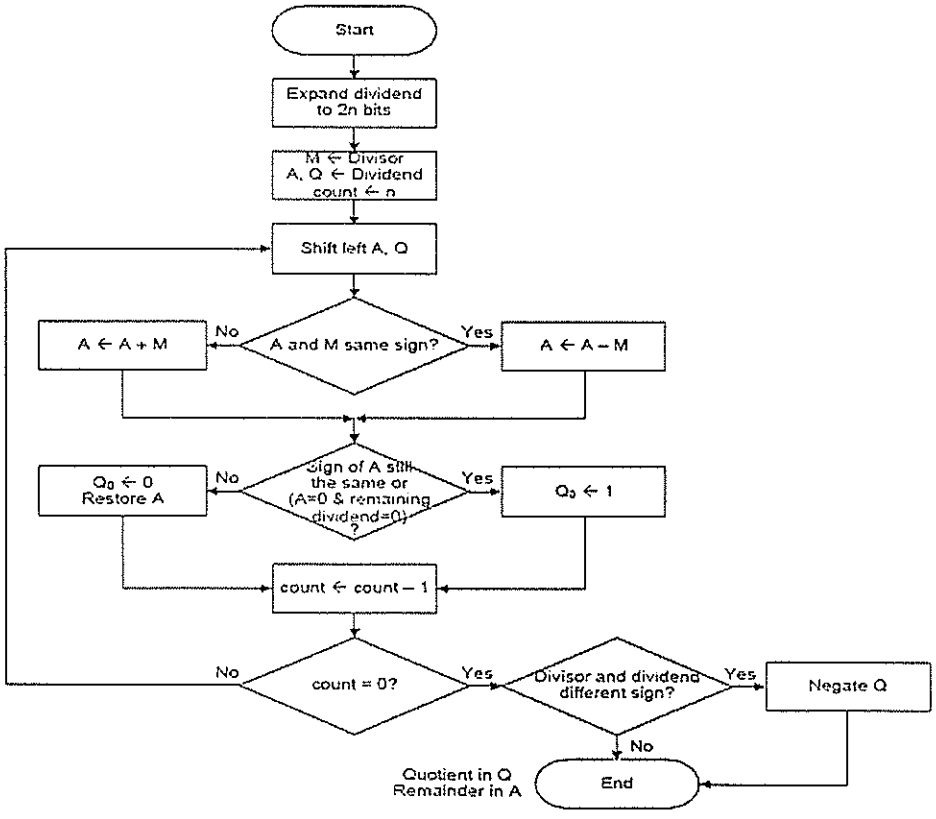
(a) Given the Booth's Algorithm flowchart:



Show the steps using Booth's Algorithm for performing the multiplication of two **4-bit two's complement** binary numbers as given below:

Multiplicand (M) = $(0101)_2$ or $(5)_{10}$
Multiplier (Q) = $(1010)_2$ or $(-6)_{10}$ [4 marks]

(b) Given the flowchart for Restoring Division Approach:



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Divide 7 / -3 in binary two's complement notation, using Restoring Division Approach. [3 marks]

(b) Assume the usage of IEEE 32-bit format for the representation of floating-point number as given below:

1	10001000	11110011111110000000000
Sign Bit (1 bit)	Biased Exponent (8 bits)	Normalized Mantissa (23 bits)

Identify the following:

i. Biased exponent value in decimal [0.5 marks]
ii. True exponent value in decimal [0.5 marks]
iii. Sign of the number [0.5 marks]
iv. Decimal equivalent of the given 32-bit floating point number [1.5 marks]

Continued ....

QUESTION 4

(a) Describe **FOUR (4)** elements that are contained in each machine instruction. [4 marks]

(b) Given the following memory values and a one-address machine with an accumulator, identify the values loaded into the accumulator by the following instructions.

Address	Values
3	25
12	38
25	54
38	86

Figure 1: Memory values

i. LOAD IMMEDIATE 3
ii. LOAD DIRECT 3
iii. LOAD INDIRECT 3
iv. LOAD IMMEDIATE 25
v. LOAD INDIRECT 12
vi. LOAD DIRECT 38

[6 x 0.5 marks = 3 marks]

(c) Explain **THREE (3)** differences between DRAM (Dynamic Random Access Memory) and SRAM (Static Random Access Memory) in terms of speed, size, and cost. [3 marks]

QUESTION 5

(a) Define **THREE (3)** characteristics of Symmetric Multiprocessor (SMP). [3 marks]

(b) Explain **THREE (3)** reasons why peripherals, such as mouse, keyboard, and printer, are not connected directly to the system bus in a computer. [3 marks]

(c) Consider a memory system that uses a 32-bit address to address at a byte level, plus a cache that uses a 32-byte line size. Assume a direct mapped cache with a tag field in the address of 20 bits.

i. Show the address format.
ii. Determine the number of addressable units.
iii. Determine the number of blocks in main memory.
iv. Determine the number of lines in cache.

[4 x 1 mark = 4 marks]

End of Paper.